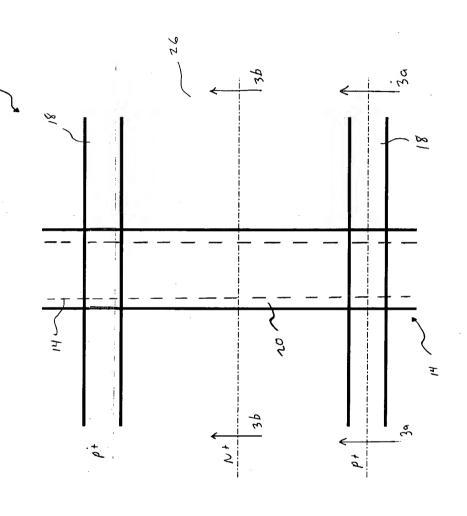


FIG. 1 (PRIOR ART)



F16. 2 (PRIOR MAT)

F16. 3b (PRIOR ART)

FOZENO Zhehnabu

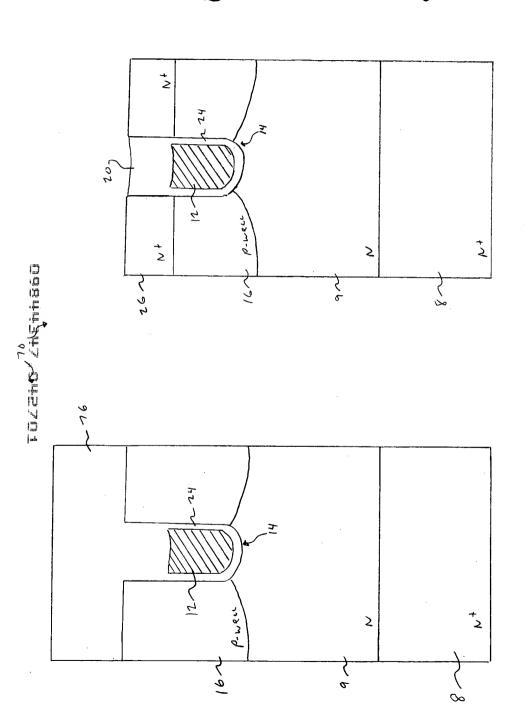
40 1 START FORMING A TRENCH IN A 42 -SEMICONDUCTOR LAYOR FORMING A GATE DIELECTRIC LAYER LINING THE TRENCH FORMING A GATE CONDUCTING LAYER 46in A loher MORTION OF THE TRENCH FORMING A DIELECTRIC LAYER 48 10 FILL AN UPPER PORTION OF THE TRENCH REMOVING PORTIONS OF THE SEMI-50~ CONDUCTOR LAYER SO THAT AL LPPER PORTION OF THE DIELECTRIC EXTENDS DUTWARDLY THEREFROM

FORMING SPACERS
LATERALLY ADJACENT
THE OUTWARDLY
EXTENDING UPPER
PORTION OF THE
DIELECTRIC LAYER

USING THE SPACERS
AS A SELF-ALIGNED
MASK FOR DEFINING
SOURCE / BODY
CONTACT REGIONS.

F16. 4

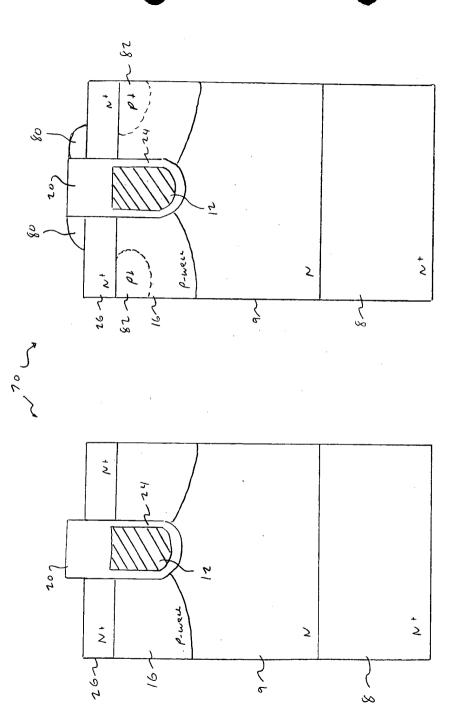
F16.6



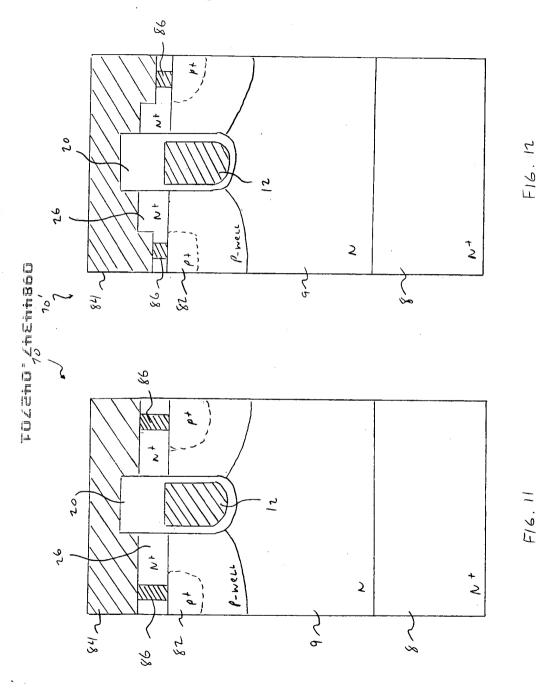
F16.8

F16.7

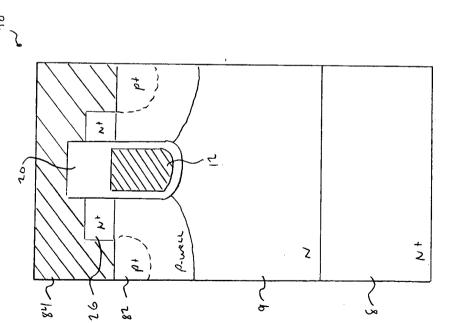
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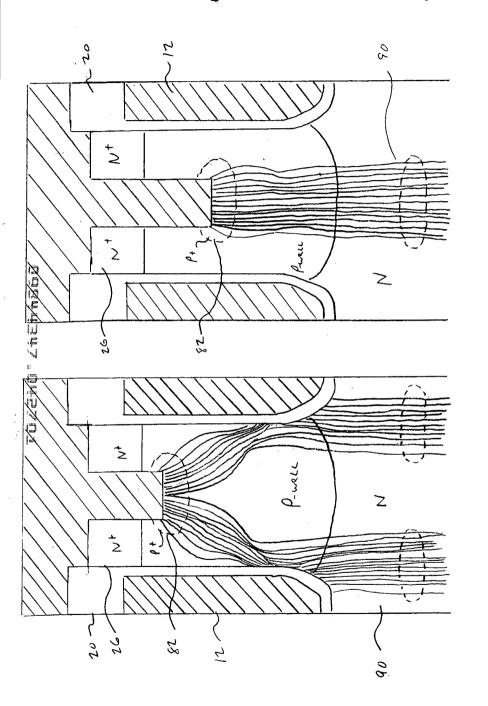
9



F16. 12



F16.1



F16. 15

F16.14